IN THE CLAIMS

1. (Currently amended) An electrically erasable programmable memory device, comprising:

a first semiconductor layer doped with a first dopant ~~in~~ at a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

a first diffusion region and a second diffusion region ~~two spaced-apart diffusion regions~~ embedded in the top side of the second semiconductor layer and defining a channel region therebetween, each diffusion region being doped with the first dopant ~~in~~ at a second concentration greater than the first concentration, ~~the two diffusion regions including a first diffusion region and a second diffusion region, a first channel region defined between the first diffusion region and the second diffusion region~~;

a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate being capable of storing electrical charge; ~~and~~

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate and separated therefrom by a first vertical insulator layer, wherein the control gate ~~being~~ is adjacent the second diffusion region and above the first

channel region and separated therefrom by a second insulator region, and wherein the control gate and the floating gate share a planarized top surface.

2. (Currently amended) The memory device of claim 1, wherein the first dopant ~~having~~ has a P-type characteristic and the second dopant ~~having~~ has an N-type characteristic.

3. (Currently amended) The memory device of claim 1, wherein the first dopant ~~having~~ has an N-type characteristic and the second dopant ~~having~~ has a P-type characteristic.

4. (Currently amended) The memory device of claim 1, wherein the first insulator region ~~having~~ has a thickness that allows tunneling of charge between the floating gate and the first channel region.

5. (Original) The memory device of claim 4, wherein the thickness is between 70 angstroms and 110 angstroms.

6. (Currently amended) The memory device of claim 1, wherein the vertical insulator is made from a silicon dioxide having a thickness that ~~provides capacitance between the floating gate and the control gate and~~ prevents leakage between the floating gate and the control gate.

7. (Currently amended) The memory device of claim 1, wherein the first vertical insulator is made from an oxide-nitrite-oxide material having a thickness that ~~provides capacitance between the floating gate and the control gate and~~ prevents leakage between the floating gate and the control gate.

8. (Original) The memory device of claim. 1, wherein the floating gate and the control gate are wrapped by a spacer.

9. (Original) The memory device of claim 1, wherein the second diffusion is in contact with a vertical connector, the vertical connector being separated from the control gate by a second vertical insulator.

10. (Currently amended) The memory device of claim 9, wherein charge is transported from the first channel region to the floating gate when a first combination of voltages ~~is~~ are applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

11. (Currently amended) The memory device of claim 10, wherein the first combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the second semiconductor layer;

applying a positive high voltage to the first diffusion region;

applying zero voltage to the second diffusion region; and

applying to the control gate a decreasing positive ~~high ramp down~~ voltage over a first time period, followed by an increasing ~~ramp up~~ voltage over a second time period ~~to the control gate~~.

12. (Currently amended) The memory device of claim 10, wherein the first combination of voltages are applied according to a method which comprises:

applying a positive voltage between 1V and ~~Vpp~~ a programming voltage to the control gate;

applying a zero voltage to the first diffusion region;

applying a positive high voltage to the second diffusion region; and

applying a positive voltage between 0V to ~~Vcc~~ a supply voltage to the second semiconductor layer.

13. (Currently amended) The memory device of claim 9, wherein charge inside the floating gate can be determined when a first combination of voltages ~~is~~ are applied to the first diffusion region, the control gate, and the second semiconductor layer.

14. (Currently amended) The memory device of claim 13, wherein the first combination of voltages are applied according to a method which comprises:

applying a ~~Vcc~~ supply voltage to the second semiconductor layer;

applying a ~~Vcc~~ supply voltage to the first diffusion region; and

applying a voltage between -2V and ~~Vcc~~ the supply voltage to the control gate.

15. (Original) The memory device of claim 1, wherein the first diffusion is in contact with a vertical connector, the vertical connector being separated from the floating gate by a second vertical insulator.

16. (Currently amended) The memory device of claim 15, wherein charge is

transported from the first channel region to the floating gate when a second combination of voltages are ~~is~~ applied to the first diffusion region, the control gate, and the second semiconductor layer.

17. (Currently amended) The memory device of claim 16, wherein the second combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a ~~Vee~~ supply voltage to the second semiconductor layer.

18. (Original) The memory device of claim 16, wherein the second combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a negative voltage to the second semiconductor layer.

19. (Currently amended) The memory device of claim 1, wherein charge is transported from the floating gate to the first channel area when a third combination of voltages ~~is~~ are applied to the second semiconductor layer, the control gate, and the first diffusion region

20. (Currently amended) The memory device of claim 19, wherein the third combination of voltages are applied according to a method which comprises:

applying a negative voltage to the control gate;

applying a high positive voltage to the second semiconductor layer; and

applying a positive high voltage to the first diffusion region.

21. (Currently amended) An electrically erasable programmable memory device, comprising:

a first semiconductor layer doped with a first dopant ~~in~~ at a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

a first diffusion region and a second diffusion region ~~two spaced-apart diffusion regions~~ embedded in the top side of the second semiconductor layer and defining a first channel region therebetween, each diffusion region being doped with the first dopant in a second concentration greater than the first concentration~~, the two diffusion regions including a first diffusion region and a second diffusion region, a first channel region defined between the first diffusion region and the second diffusion region~~;

a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate capable of storing electrical charge ~~and having at~~

~~least two lateral sides~~; and

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate on ~~and surrounding~~ at least two sides of the floating gate and separated therefrom by a vertical insulator layer, the control gate being disposed above the first channel region and separated therefrom by a second insulator region.

22. (Currently amended) The memory device of claim 21, wherein the first dopant ~~having~~ has a P-type characteristic and the second dopant ~~having~~ has an N-type characteristic.

23. (Currently amended) The memory device of claim 21, wherein the first dopant ~~having~~ has an N-type characteristic and the second dopant ~~having~~ has a P-type characteristic.

24. (Currently amended) The memory device of claim 21, wherein the first insulator region ~~having~~ has a thickness that allows tunneling of charge between the floating gate and the first channel region.

25. (Original) The memory device of claim 24, wherein the thickness is between 70 angstroms and 110 angstroms.

26. (Currently amended) The memory device of claim 21, wherein the vertical insulator is made from a silicon dioxide having a thickness that ~~provides capacitance between the floating gate and the control gate and~~ prevents leakage between the floating gate and the control gate.

27. (Currently amended) The memory device of claim 21, wherein the first vertical insulator is made from an oxide-nitrite-oxide material having a thickness that ~~provides capacitance between the floating gate and the control gate and~~ prevents leakage between the floating gate and the control gate.

28. (Currently amended) The memory device of claim 21, wherein the control gate ~~are~~ is wrapped by a spacer.

29. (Original) The memory device of claim 21, wherein the second diffusion is in contact with a vertical connector, the vertical connector being separated from the control gate by a second vertical insulator.

30. (Currently amended) The memory device of claim 29, wherein charge is transported from the first channel region to the floating gate when a first combination of voltages ~~is~~ are applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

31. (Currently amended) The memory device of claim 30, wherein the first combination of voltages are applied according to a method which ~~comprises~~:

applying a positive high voltage to the second semiconductor layer;

applying a positive high voltage to the first diffusion region;

applying zero voltage to the second diffusion region; and

applying to the control gate a positive decreasing ~~high ramp down~~ voltage for a first time period, followed by an increasing ~~ramp up~~ voltage for a second time

period ~~to the control gate~~.

32. (Currently amended) The memory device of claim 30, wherein the first combination of voltages are applied according to a method which comprises:

applying a positive voltage between 1 V and ~~Vpp~~ a programming voltage to the control gate;

applying a zero voltage to the first diffusion region;

applying a positive high voltage to the second diffusion region; and

applying a positive voltage between 0V to ~~Vcc~~ a supply voltage to the second semiconductor layer.

33. (Currently amended) The memory device of claim 29, wherein charge inside the floating gate can be determined when a first combination of voltages ~~is~~ are applied to the first diffusion region, and the control gate.

34. (Currently amended) The memory device of claim 33, wherein the first combination of voltages are applied according to a method which comprises:

applying a ~~Vcc~~ supply voltage to the second semiconductor layer; applying ~~a~~ ~~Vcc~~ the supply voltage to the first diffusion region; and

applying a voltage between -2V and ~~Vcc~~ the supply voltage to the control gate.

35. (Original) The memory device of claim 21, wherein the first diffusion is in

contact with a vertical connector, the vertical connector being separated from the floating gate by a second vertical insulator.

36. (Currently amended) The memory device of claim 35, wherein charge is transported from the first channel region to the floating gate when a second combination of voltages ~~is~~ are applied to the first diffusion region, the control gate, and the second semiconductor layer.

37. (Currently amended) The memory device of claim 36, wherein the second combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the control gate; applying a negative voltage to the first diffusion region; and

applying a ~~Vcc~~ supply voltage to the second semiconductor layer.

38. (Currently amended) The memory device of claim 36, wherein the second combination of voltages are applied according to a method which comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a negative voltage to the second semiconductor layer.

39. (Currently amended) The memory device of claim 21, wherein charge is transported from the floating gate to the first channel area when a third combination of voltages ~~is~~ are applied to the second semiconductor layer, the control gate, and the first

diffusion region

40. (Currently amended) The memory device of claim 39, wherein the third combination of voltages are applied according to a method which comprises:

applying a negative voltage to the control gate;

applying a high positive voltage to the second semiconductor layer; and

applying a positive high voltage to the first diffusion region.

41-49 (canceled).